The CELL Architecture and Applications

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Overview

1. Introduction into the CELL architecture
2. Today's CELL applications
3. Video Processing on CELL

EuTEC-VTD R&D contribution to products

SONY´s 1st LCD TV (2000)

- Motion adaptive de-interlacing algorithm
- ***Software solution on TriMedia***

European high end CRT (2003)

- ***PiCTURE****Power*™
  - Motion-compensated 100Hz up-conversion
  - 3D-noise reduction + Picture Improvement
- ***First software based TV platform***
- Hybrid: Two co-processor ASICs and DSP algorithms
- TriMedia / Viper

VAIO Product Line (since 2004)

- EuTEC ***Motion Reality LE*** in VAIO Products worldwide
- Offers best video quality in today's PC market
- x86 Architecture

EuTEC-VTD R&D contribution to products

Digital Still Camera (2005)

- Algorithms for Noise Reduction
- Algorithm Model Development

Wega Engine 2006

- Segmentation algorithm for picture improvement
- Noise Measurement
- Reference model and hardware design

CELL: Blu-ray Player / Game Library

- Video Post Processing library
- High optimization for full HD processing

2005/2006/2007: High Frame Rate Project

- Algorithm Development for MCFC
- ASIC for WXGA model and FHD model

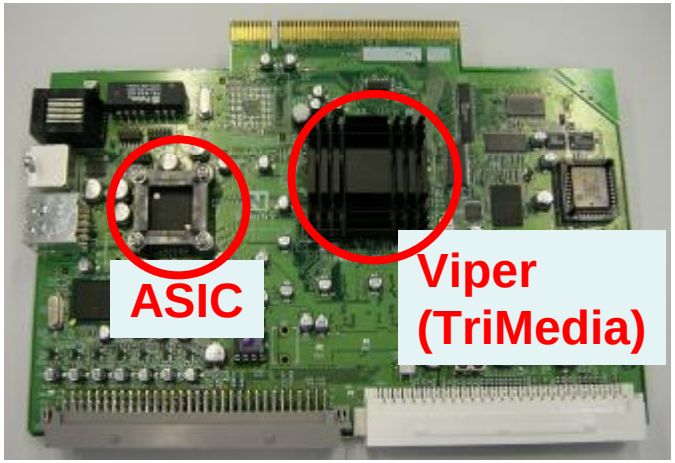
2003: Sonys first „ Software TV“ in Europe

- **Advantages:**
  - less components
  - flexbile configurations
  - „rapid prototyping“

KV-32HQ100

Problem: **DSP performance**

Solution: **Hybrid system (ASIC + DSP)**



The CELL Architecture

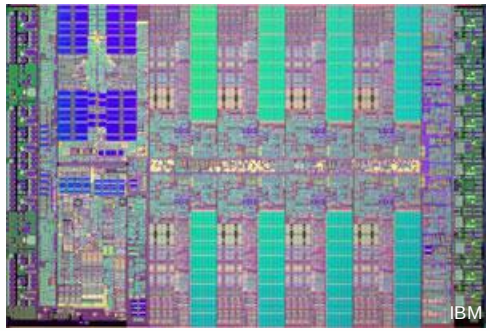
Kutaragi-san (Sony Computer Entertainment, ~2001):

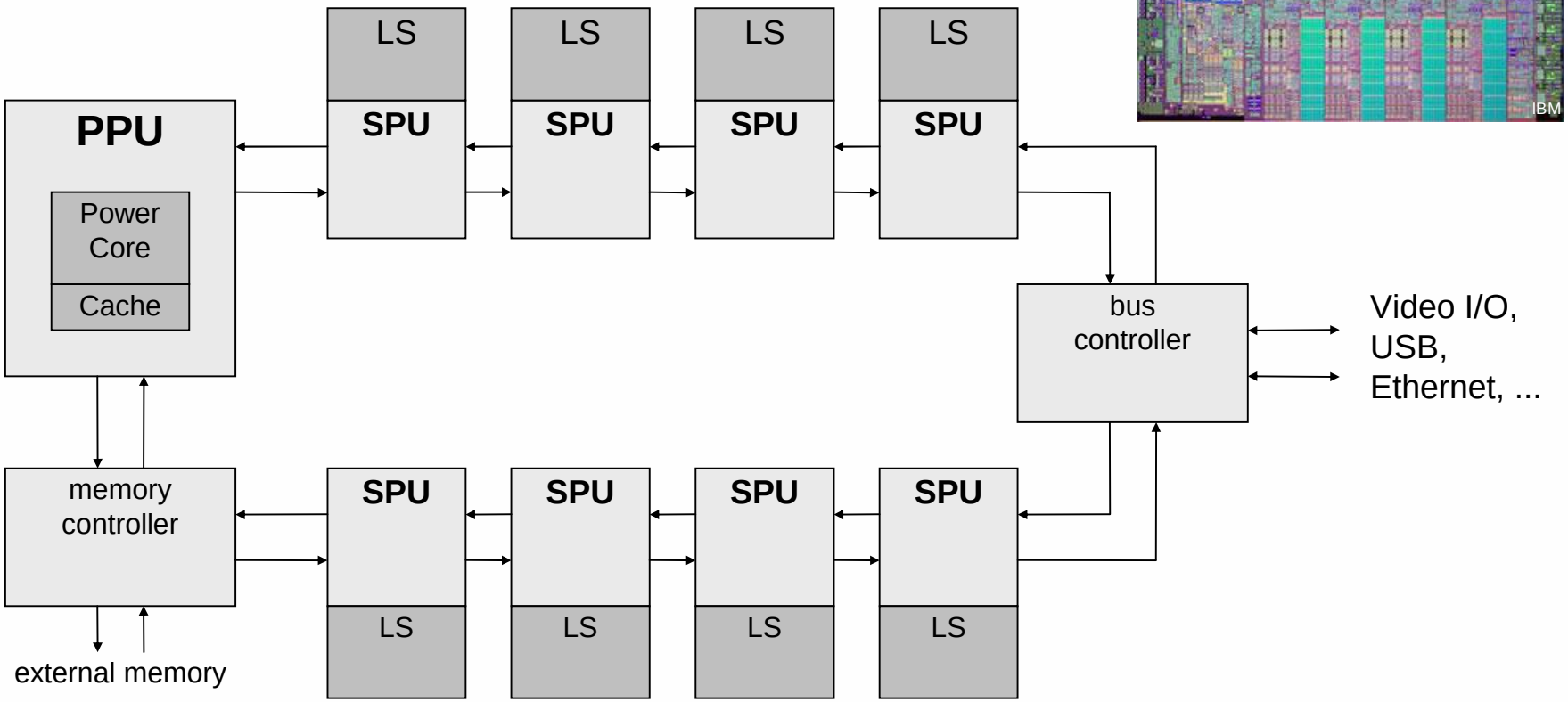
„Let‘s develop a chip, which is 1000 times faster than current graphics / multimedia processors“

→ CELL architecture
by IBM, Sony and Toshiba

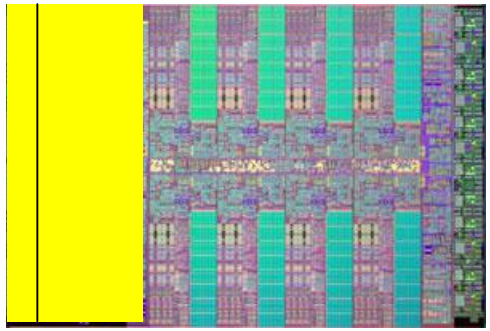
CELL block diagram

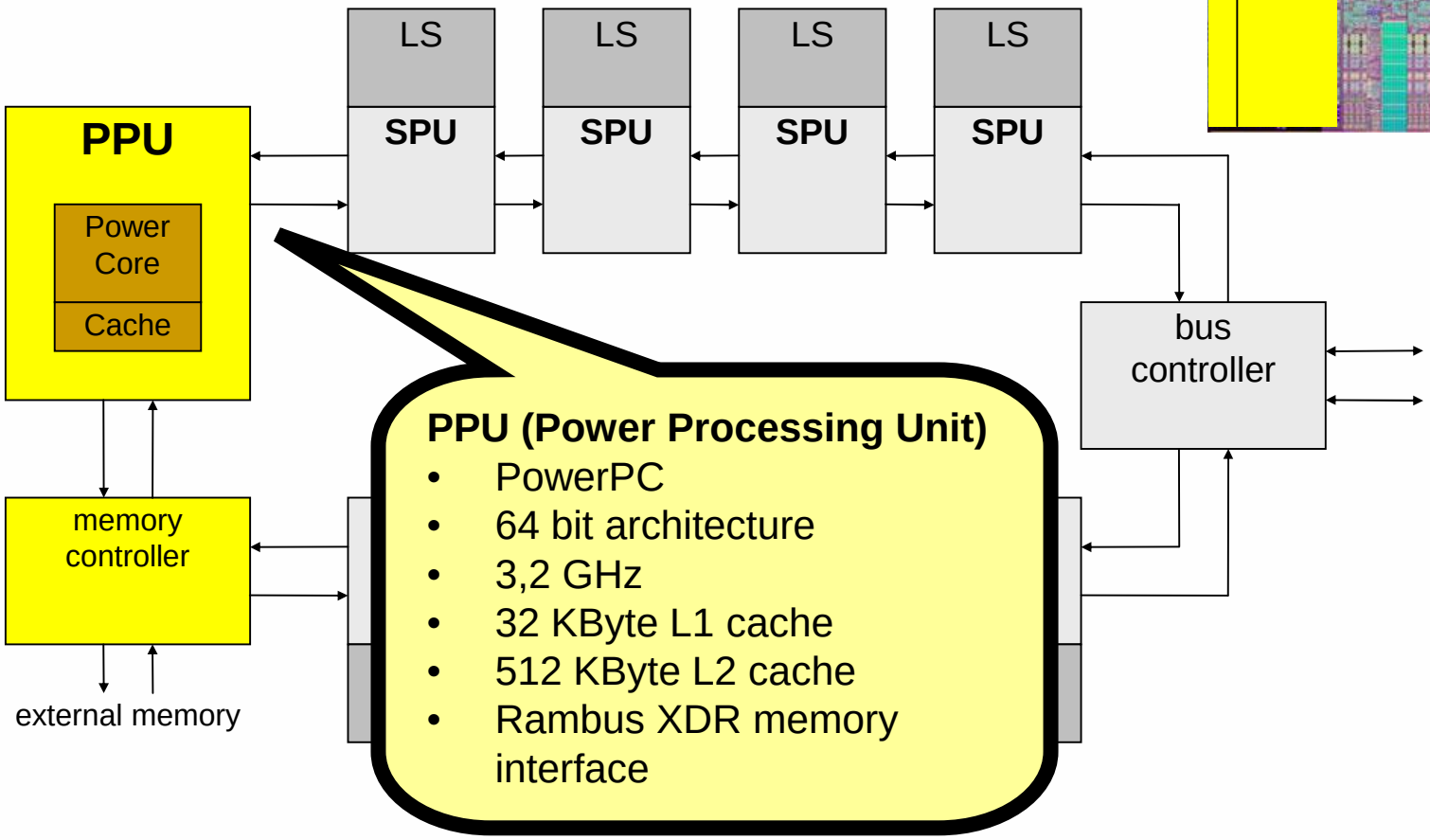
- **9 processors in one package**





CELL block diagram: PPU

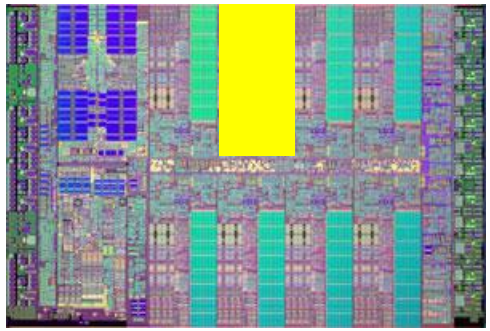


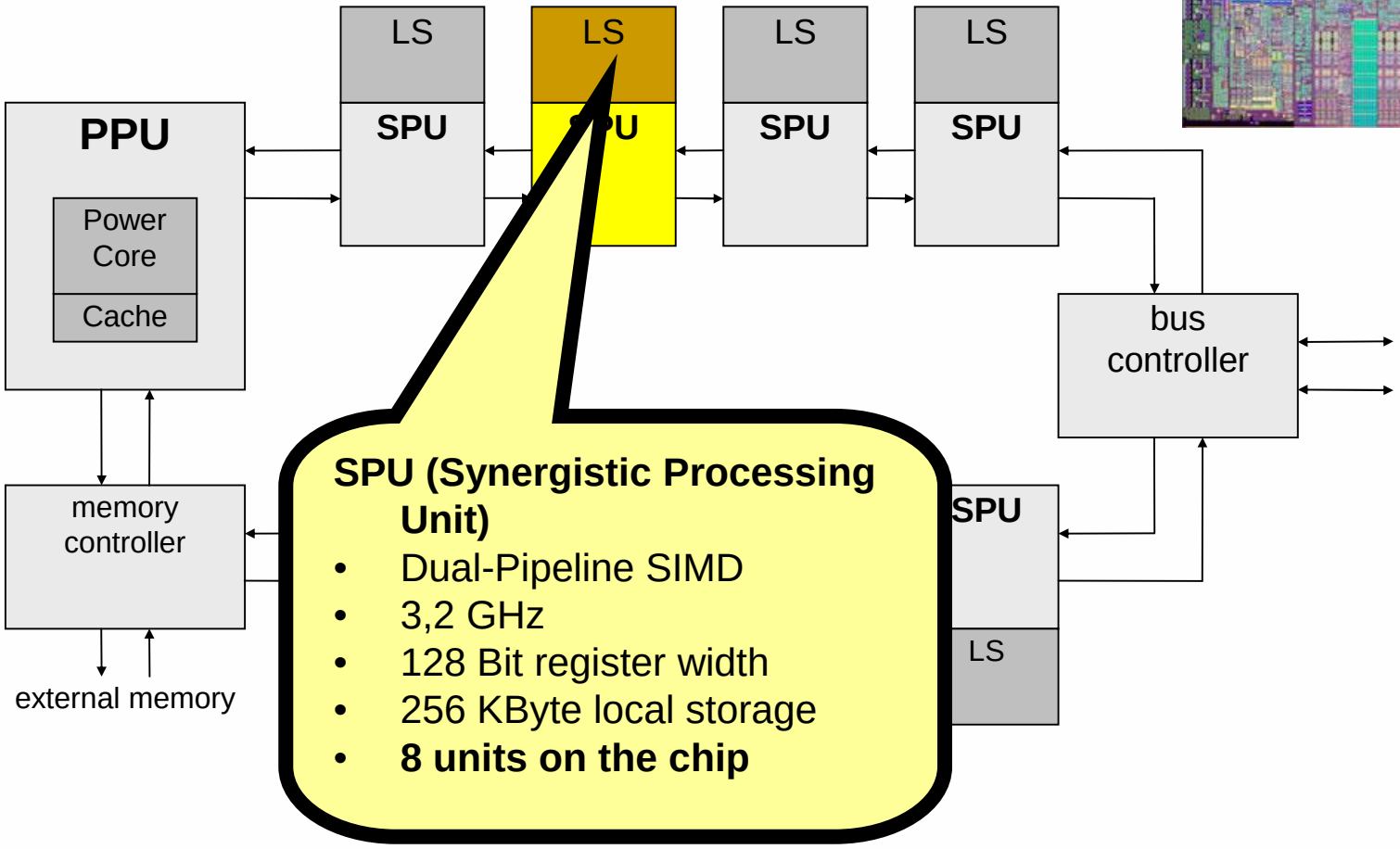


PPU (Power Processing Unit)

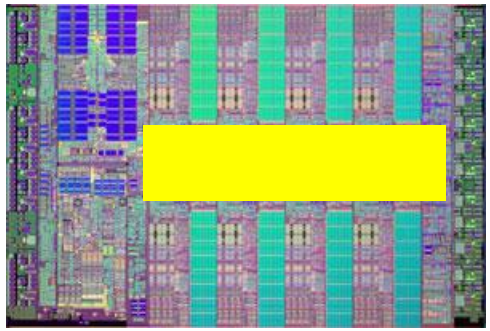
- PowerPC
- 64 bit architecture
- 3,2 GHz
- 32 KByte L1 cache
- 512 KByte L2 cache
- Rambus XDR memory interface

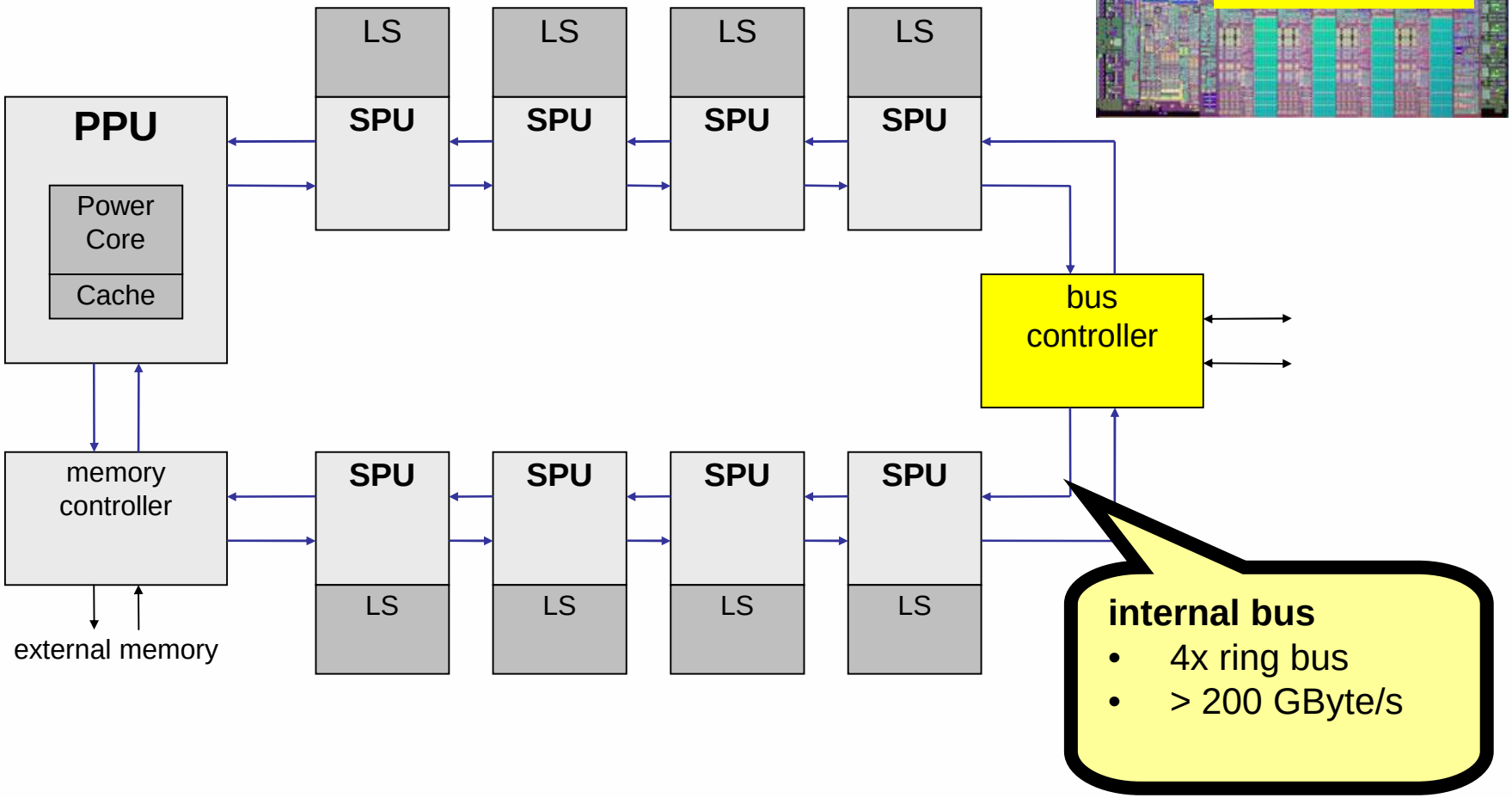
CELL block diagram: SPU





CELL block diagram: bus



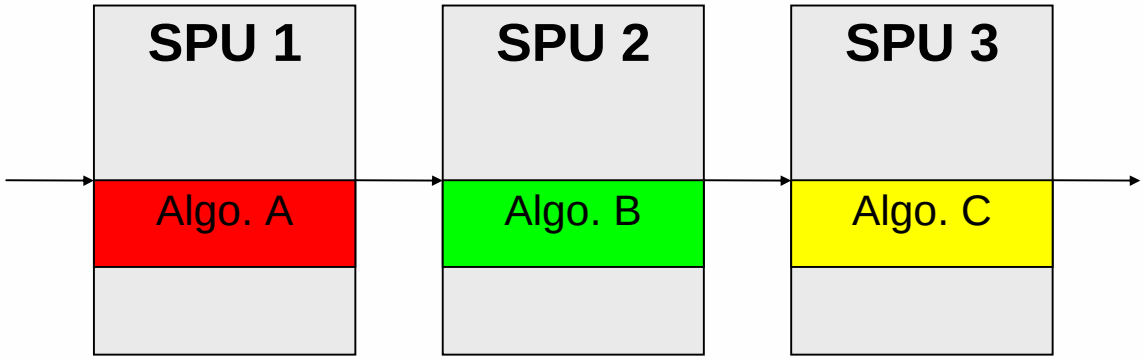


Three levels of parallelism in one chip

1. processors
2. instructions
3. data

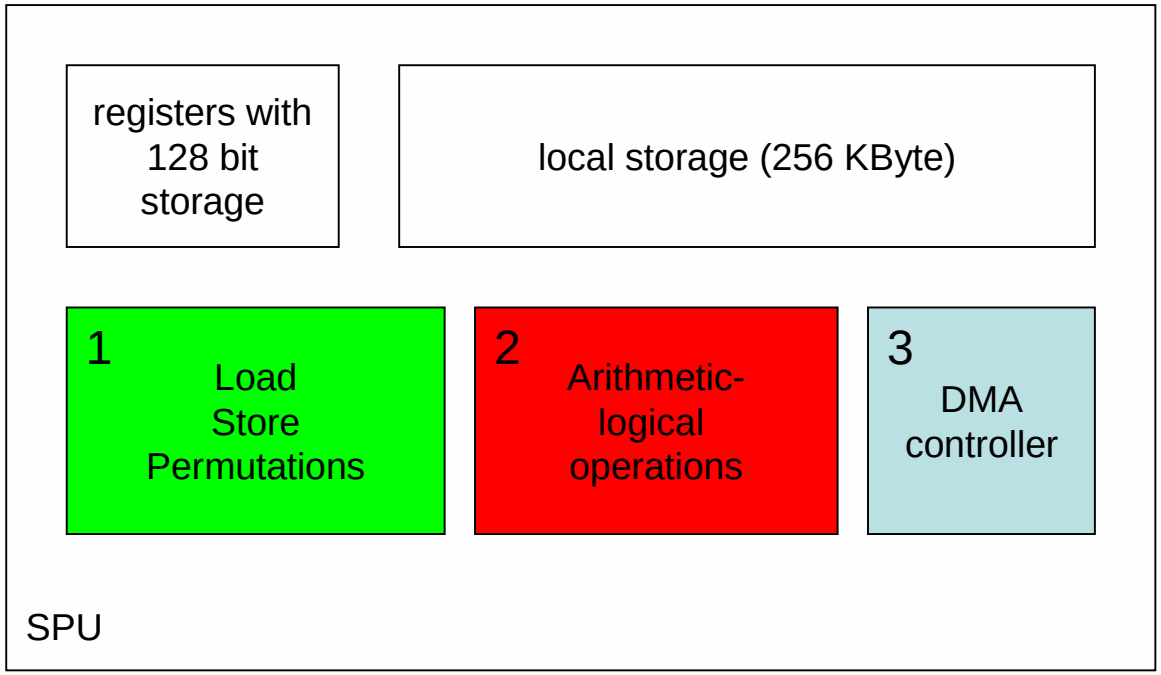
Parallelisation on multiple processors

- **Distribute algorithms over several processors**
- **Could be multiple SPUs, or SPUs+PPU**



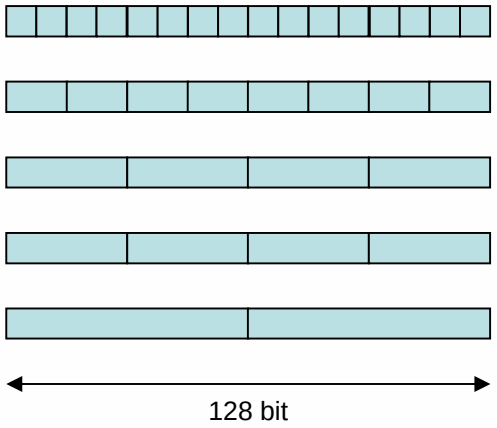
Parallelisiation on instruction level

- **Each SPU has 2 parallel instruction paths**
- **asynchronous DMA is possible**



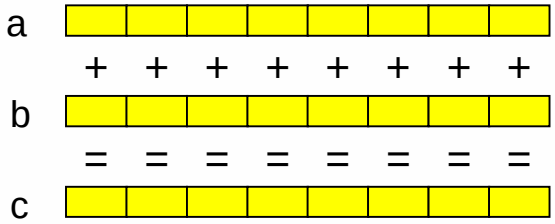
Data Level Parallelisation

- **128 Bit SIMD architecture**
  - 16 * Byte
  - 8 * Short
  - 4 * Integer
  - 4 * Single Precision Float
  - 2 * Double Precision Float



Example: c = a + b

→ `c = spu_add(a,b)`



Today's CELL Applications

CELL platforms

- **Sony OS on PS3**
  - used by Game Developers
  - good support by Sony
  - includes many easy-to-use libraries (audio/video codecs, I/O drivers ...)
  - full system access including RSX

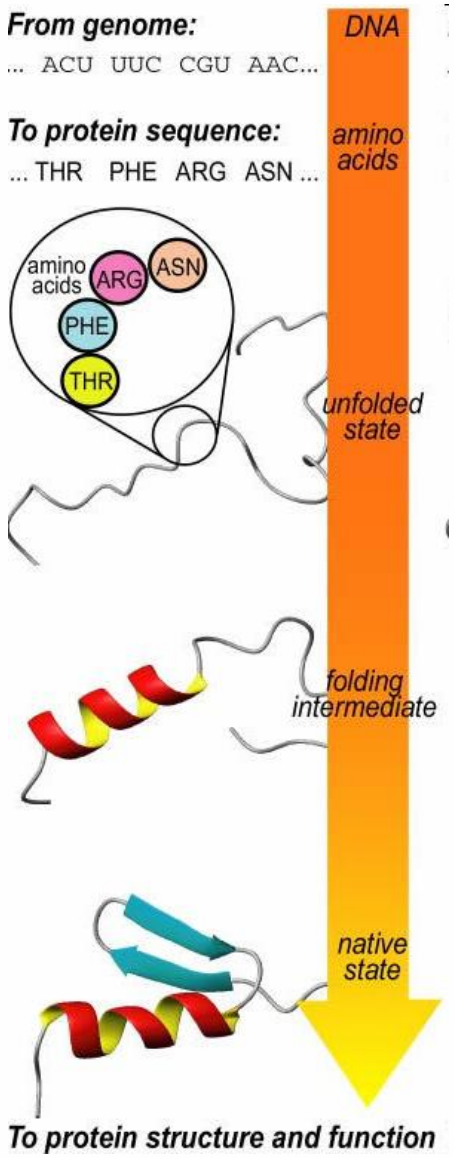
- **Linux on PS3**
  - no Sony developer support
  - restricted system access
  - no libraries included, but extensible

- **IBM Dual CELL Blade**
- **Mercury PCI Accelerator Board**

Number crunching on CELL

Folding@home distributed computing

- **Stanford university project**
  - Calculation of protein foldings for the research of Alzheimer, Parkinson and Cancer
- **Project runs since year 2000, mainly on Intel CPUs**
- **Sony PS3 joined in 2006**



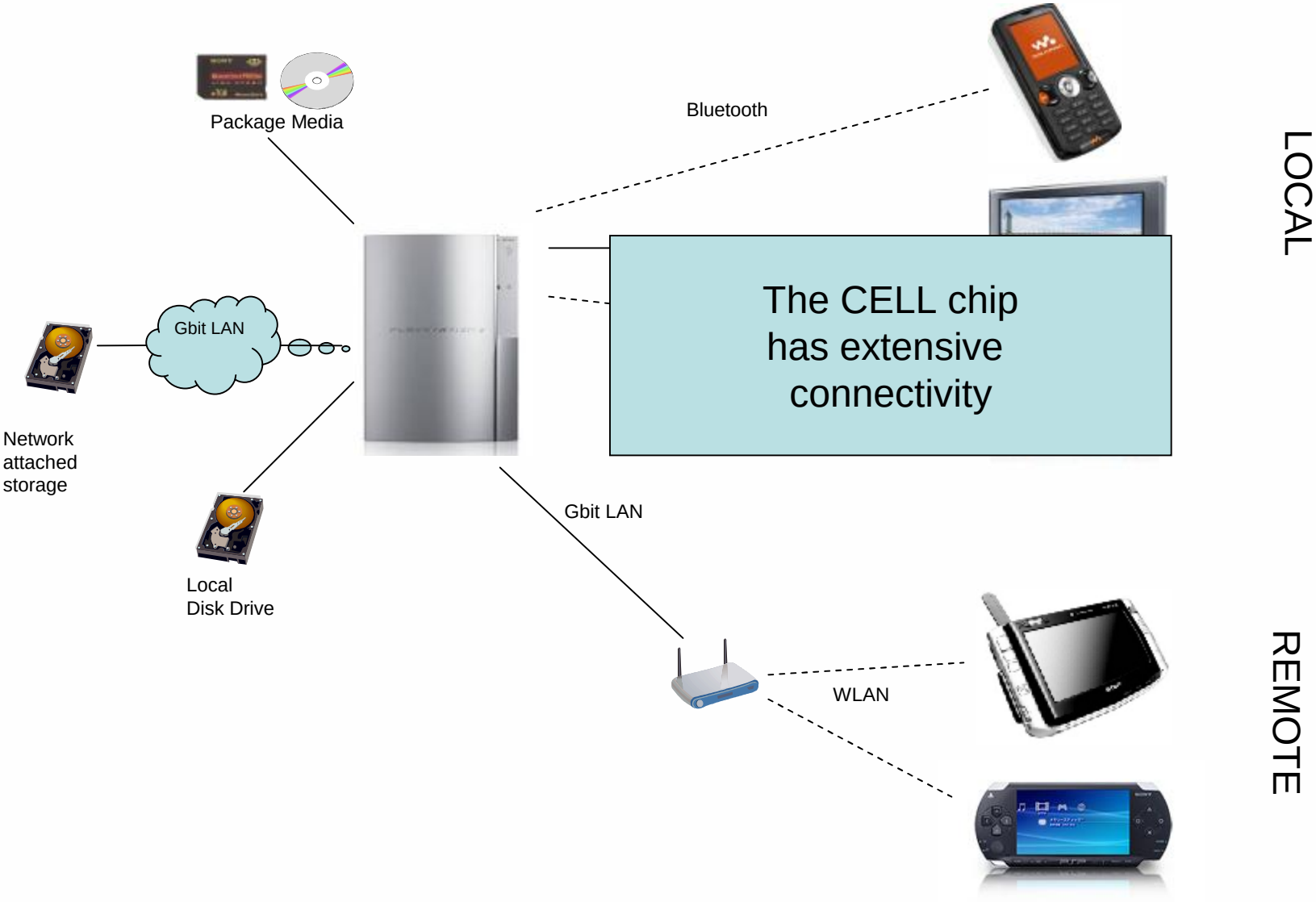
- **Statistics** **(29 May 2007)**

OS	Achieved TFlops	Processors
Windows	186	1,712,355
Linux	42	228,944
PS3	602	139,659

Video Processing on CELL

Streaming Server
Streaming Client

CELL as streaming server



CELL as streaming client

Problem: Video streams have very different properies

- Codecs (MPEG1 – MPEG4/AVC)
- Frame Rate <15Hz – 120 Hz
- Resolution <320x240 – 1920x1080
- Raw data rate 20 Mbit/s – 4 GBit/s

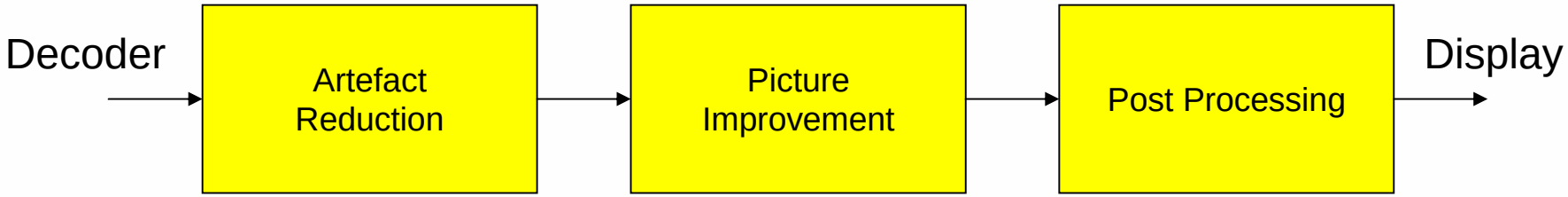
→ flexible architecture needed

CELL as streaming client

- Decryption
- Decoding
- De-Interlacing
- Sharpness Enhancement
- Block Noise Reduction
- Frame Rate Conversion
- Scaling
- Colour Space Conversion

→ Sony Stuttgart activities

Video Processing System Overview



Noise Reduction
...

De-Interlacing
Frame Rate Conversion
...

Scaling
...

Artefact Reduction

- **Compression causes artefacts in the stream**
  - blocking
  - ringing
  - ...
- **Artefacts depend on the codec**

Block Noise Reduction
Error Concealment

- **Stream may have had bad quality before streaming**
  - low contrast due to bad illumination
  - low sharpness, blurring
  - noise
  - shaky camera motion
  - ...

Contrast Enhancement
Sharpness Enh.
Noise Reduction
...

→ Flexible artefact reduction algorithms needed

Picture Improvement

- **Frame rate in video stream may differ from display rate**
  - Internet Streams (variable frame rate)
  - Digital Still Camera videos (15 Hz)
  - 24p film material
  - NTSC video (60Hz) in PAL regions (50Hz)

- **Algorithms**
  - Frame Drop / Repeat → small displays
  - Blending → small/medium displays
  - Motion Compensation → large displays

→ Flexible picture improvement algorithms needed

Demo: Frame Rate Conversion

- **Demo**

Post Processing

- **Streams must be adapted to the display‘s properties**

- **Scaling**
  - Pixel Repetition for small changes
  - Bilinear/Bicubic for medium size changes
  - Polyphase for strong downscaling
  - Super Resolution Algorithms for strong upscaling

- **Display adaptive post-processing**
  - chroma processing
  - ...

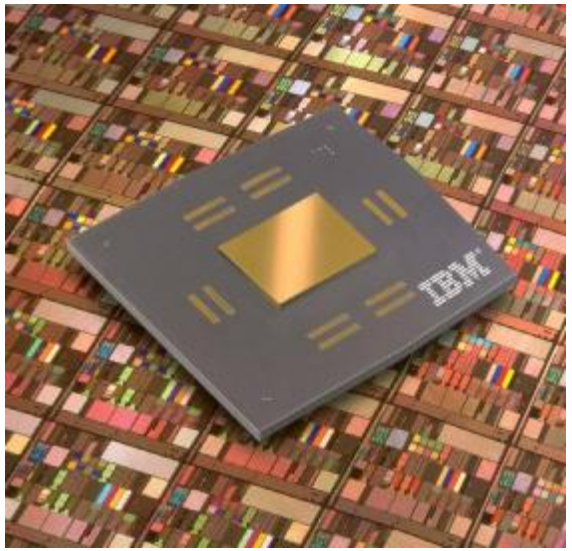
→ Flexible post processing algorithms needed

CELL Power

- **Processing Power**
  - CELL is 15x faster than Pentium 4 processors
  - CELL has 4x bandwidth of PCI-Express
  - SPUs are very suitable for streaming applications
  - Hardware fits well to a flexible architecture

- **But:**
  - Multi-Processor system requires communication overhead
  - SIMD architecture is only optimal for aligned data
  - Memory access is difficult due to small SPU storage

Summary



CELL provides high performance for real-time signal processing of large data sets

+ **flexible software architecture**
+ **fast (>3 Ghz, 8 parallel processors)**
+ **freely available development enviroment**
+ **easily accessible hardware**

- **programming is complex**
- **power consumption**

References

- **IBM Broadband Engine Resource Center**
  - http://www-128.ibm.com/developerworks/power/cell
- **Sony CELL information site**
  - http://cell.scei.co.jp
- **Barcelona Supercomputing Center**
  - http://www.bsc.es/projects/deepcomputing/linuxoncell