Background
Data traffic in the Internet is continuously growing. Furthermore, always new protocols and protocol extensions are being developed in order to provide new services. Hence, packet processing systems on the line cards of network nodes have to be capable to process some 100 million packets per second in the future and still shall allow to be easily adaptable to new functional requirements. Network processors or FPGAs are currently used for this.

At the Institute of Communication Networks and Computer Engineering, we designed an FPGA-based, modular packet processing architecture and built it up as a prototype system. The architecture combines the advantages of network processors and FPGAs. One can describe a packet processing task at register-transfer level (RTL) in VHDL using an RTL module or program it in software using a processor module.

Task
In this student thesis a novel processor module shall be developed. This module shall implement a "synchronous data flow (SDF) architecture", where a pipeline of many processing engines (PEs) continuously processes the data that flows through it. The thesis contains the following steps:

- Becoming familiar with the concept of synchronous dataflow architectures
- Design of a specific SDF architecture taking into account the constraints of packet processing tasks
- Implementation of the SDF architecture and integration into the given prototypical packet processing system
- Operation and test on the FPGA-based Universal Hardware Plattform

Requirements
Computer Engineering I
Digital systems design

Desirable knowledge
Communication Networks I
Communication Networks II
Computer Engineering II

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